Si$_3$N$_4$ on GaAs by direct electron cyclotron resonance plasma assisted nitridation of Si layer in Si/GaAs structure


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Si$_3$N$_4$ has been produced on GaAs with low interface trap densities by electron cyclotron resonance N$_2$–He plasma assisted nitridation of a Si layer deposited on a GaAs (100) substrate. Nitridation at 150 and 400 °C was monitored by x-ray photoelectron spectroscopy (XPS) and produced stoichiometric Si$_3$N$_4$. The nitride layer thickness, as determined from XPS as a function of photoelectron takeoff angle, initially increased rapidly with nitridation time with a transition at a thickness of 12–18 Å to slower growth. Capacitance/voltage and conductance/angular frequency measurements were performed on metal-insulator-semiconductor capacitors fabricated from the nitrided samples. The results demonstrated interface trap densities with a minimum of 3.0 $\times 10^{11}$ eV$^{-1}$ cm$^{-2}$ when nitrided at 150 °C. At 400 °C the nitridation produced a poor quality interface, which resulted either from the higher temperature or from nitridation of all of the Si, leaving the Si$_3$N$_4$ in direct contact with the GaAs. © 1998 American Vacuum Society.

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I. INTRODUCTION

GaAs is an excellent candidate material for high speed electronic devices owing to its high electron mobility (about six times the electron mobility of silicon). The main challenge preventing the application of GaAs in such devices is the lack of a suitable insulator to implement the metal-insulator-semiconductor field-effect transistor (MISFET). Unlike those of Si, the native oxides of GaAs have not been found stable, nor to be suitable dielectrics. Intensive research has been devoted to solving this problem. One of the most promising of the candidate insulators is silicon nitride, primarily because it is an excellent ion diffusion barrier and because corrosion reactions with GaAs surface are not observed. To date, however, electrical performances of Si$_3$N$_4$ dielectrics on GaAs comparable to those of SiO$_2$ on Si have not been reported. The poor performance of Si$_3$N$_4$/GaAs structures is caused mainly by high ($>10^{12}$ eV$^{-1}$ cm$^{-2}$) interfacial trap state densities.

Examination of previous reports on processes forming Si$_3$N$_4$/GaAs interfaces suggests that damage to the GaAs surface occurred during nitride deposition. For example, thermal nitridation of pre-deposited silicon, only possible at temperatures higher than 1000 °C, and chemical vapor deposition (CVD) using silane and ammonia at 700–900 °C would both result in arsenic loss and a consequent increase in dangling bonds at the interface. An attempt has been made to improve the interface by using plasma-enhanced chemical vapor deposition (PECVD) at 200–300 °C. Unfortunately, energetic species from the plasma are likely to have damaged the GaAs surface, and again the interface was found to have degraded. Finally, remote plasma-enhanced chemical vapor deposition (RPECVD) was used to reduce plasma damage, by separating the plasma by at least one mean free path from the semiconductor surface. Nevertheless, GaAs surface degradation was observed.

In this article, we report on an improved approach in which a GaAs surface was coated with a thin layer of Si which was subsequently converted to Si$_3$N$_4$ by RPECVD nitridation. This permits the nitride to be formed without damage to the GaAs using a low process temperature. For this purpose, a nitrogen–helium plasma was used for nitridation of the silicon layer pre-grown using a low power electron cyclotron resonance (ECR) plasma on p$^+$-GaAs (100). The plasma conditions for pure silicon deposition were reported to be free of damage induction on the GaAs surface. Successful attempts at thermal nitridation of silicon under an ammonia atmosphere have been reported in the literature, but nothing about ECR plasma assisted nitridation of silicon on GaAs under nitrogen–helium atmosphere has so far appeared.

II. EXPERIMENTS

All experiments described were carried out in a multi-chamber ultrahigh vacuum (UHV) deposition system described in detail elsewhere. The facility includes conventional and gas source molecular beam epitaxy (GS-MBE) chambers, electron cyclotron resonance microwave plasma-enhanced chemical vapor deposition (ECR-CVD), and x-ray photoelectron spectroscopy (XPS). All deposition and analysis facilities are connected through ultrahigh vacuum transfer tubes (residual pressure $<5.0 \times 10^{-10}$ Torr). The Zn-doped p$^+$-GaAs (100) substrates were etched for 40 s in HCl, rinsed in flowing de-ionized water for 3 min, blown dry in dry N$_2$, bonded to a Mo block with In paste, and loaded into the GS-MBE chamber through the introduction chamber of...
the UHV system. The substrate was annealed at 600 °C under an arsenic flux to desorb the native oxide. The surface reconstruction was monitored using reflection high energy electron diffraction (RHEED) and was (2×4) after completion of the oxide removal. Surface cleanliness was verified by XPS. Epitaxial 1 μm thick Be-doped (~5.0 ×10¹⁶ cm⁻³) p⁺-GaAs was grown following the procedures described elsewhere. The surface was again characterized by XPS and transferred to the CVD chamber for silicon layer growth.

The Si was deposited at 330 °C using a low power (60 W) remote SiH₄–He plasma. The chamber pressure during deposition was 1.4×10⁻⁴ Torr, with partial pressures of 5.5 ×10⁻⁵ Torr for SiH₄ and 8.5×10⁻⁵ Torr for He. These deposition conditions have been found to be noncorrosive to the GaAs surface. To initiate the plasma, the chamber pumping rate was reduced allowing the gas pressure to rise until the plasma ignited. The pumping rate was then increased until a satisfactory plasma was obtained. The Si deposition rate was ~0.3 Å/s, and the deposition time was 90 s. The deposition layer thickness was ~30 Å, as determined by XPS. No contaminant species were detected by XPS in or on the Si layers before nitridation.

Nitridation was performed at 400 and 150 °C, using a 350 W N₂–He ECR remote plasma in the CVD chamber. The plasma-to-substrate distance was ~35 cm. Because the microwave plasma interfered with the thermocouple measurement, it was not possible to directly read or control the substrate temperature during nitridation. Hence, the substrate heater power was set manually to provide the desired temperature before initiation of the plasma, and no adjustment was made during nitridation. When the plasma was turned off, the thermocouple suggested that the substrate temperature may have risen as much as 100 °C due to plasma heating. The total pressure was 2.4×10⁻⁴ Torr consisting of 1.5×10⁻⁴ Torr of N₂ and 9×10⁻⁵ Torr of He. The nitridation was interrupted and the resulting nitride was characterized by XPS periodically. The total nitridation time was 25 min (1500 s). Using atomic sensitivity factors determined by analysis of Si and stoichiometric Si₃N₄ and consistent with standard values, the resulting nitrides were determined to be stoichiometric. The thickness of nitride was obtained from the intensity ratio of Si 2p peak of pure Si and that of Si in the nitride environment.

For electrical measurements, the Si₃N₄ formed by nitridation of 30 Å of Si on GaAs was overcoated with 270 Å thick Si₃N₄, grown as described elsewhere. The samples then were cut into pieces and subjected to various rapid thermal annealing (RTA) treatments. Aluminum top electrodes were evaporated and photolithographically patterned to form 300 μm diameter MIS capacitors.

III. RESULTS AND DISCUSSIONS

Photoelectron spectra obtained between 97 and 110 eV binding energies showed as-deposited 30 Å Si to exhibit only the ~99 eV peak associated with valence 0 (elemental) Si and Ga 2p peaks at ~104 and ~108 eV. After nitridation a peak at ~102 eV was found, which is due to Si⁺⁺ in Si₃N₄. From the evolution of the peak areas and heights recorded at several angles between 20° and 70° with respect to the sample normal, the thickness of the nitride and the elementary Si layers was estimated. Figure 1 presents the evolution of the resulting Si₃N₄ thickness as a function of nitridation time. The results indicated initial fast growth of the nitride followed by a transition to slower growth. A similar process has been found in thermal and ion beam nitridation of silicon. The process in the higher temperature sample was faster than the one in the low temperature sample, probably due to the effect of temperature enhancement in the nitridation kinetics. In fact, high temperature enhances the mobility of ions and excited nitrogen species, so that they can move deeper into the silicon layer against the diffusion barrier created by the previous nitrided layers. According to the curves in Fig. 1, an extrapolation over 25 min (1500 s) suggests a complete nitridation of 30 Å (thick silicon layer) for the sample nitrided at high temperature and a possibility of some (2–3) remaining non-nitrided Si monolayers for the sample at low temperature.

C–V characteristics of capacitors on Si₃N₄ nitrided at the nominal temperature of 400 °C and subsequently annealed at 550 °C for 15 s under N₂ are shown in Fig. 2(a). Curves (not presented in this article) from other pieces of sample annealed at other temperatures showed degraded performances. A hysteresis of 300 mV was observed at 1 MHz and 150 mV at 1 kHz with voltages swept from 2 to ~3.5 V. The ''frequency dispersion'' is defined here according to practice based on the voltage difference between C–V curves measured at 1 MHz and 1 kHz C–V at a capacitance equal to the flat band value Cₐ. The relatively large hysteresis indicates negative charge trapped in deep states at the dielectric/semiconductor interface. The large frequency dispersion shows strong Fermi level pinning away from the conduction band minimum. These facts and the lack of significant accumulation were consistent with the poor quality dielectric/GaAs interface.
The electrical measurements were also carried out for the sample which was nitrided at a nominal temperature of 150 °C. Optimal electrical properties were obtained on the piece of the sample postnitridation annealed at 650 °C for 15 s. The C–V characteristics of the resulting capacitor are shown in Fig. 2(b). The hysteresis was <50 mV for both 1 MHz and 1 kHz C–V curves, and the frequency dispersion is near zero. The quasistatic C–V curve performed on this sample shows normal accumulation, depletion, and inversion. From the conductance loss characteristic, \((G/\omega)\) versus angular frequency \((\omega)\), we extracted the density of interface states \(D_{it}\) for the sample nitrided at low temperature using the following relation:

\[
D_{it} = \left( \frac{G}{\omega} \right)_{\text{Max}} \frac{f_{D}(\sigma_{s})qA}{\left[ f_{D}(\sigma_{s})qA \right]^{-1}},
\]

where \(f_{D}\) is a universal function of the standard deviation of band bending \((\sigma_{s})\) and \(A\) is the area of the capacitor. The values of \(f_{D}\) used here have been reported elsewhere.\(^{24}\) A minimum conductance peak of 5.2 pF (Fig. 3) is obtained at a gate bias of \(-0.40\) V and corresponds to \(D_{it} \approx 3 \times 10^{11}\) eV\(^{-1}\) cm\(^2\) at the center of the GaAs energy gap (see Fig. 4).

IV. CONCLUSION

Based on the XPS results, the low temperature nitridation converted \(-90\%\) of the Si surface layer to Si\(_3\)N\(_4\), leaving 1 or 2 ML of Si separating the GaAs from the nitride. This produced the lowest density of interface states, while still providing adequate capacitor performance. This result is similar to the one obtained on Si\(_3\)N\(_4\)/Si/GaAs by Mui et al.\(^{25}\) The higher temperature nitridation converted a larger fraction of Si to Si\(_3\)N\(_4\) and produced poorer performance. Results to date have not allowed a definitive conclusion about why the higher temperature was unsuccessful. Corrosion of the GaAs interface was not observed in XPS data, nor were peaks associated with GaN present in any spectra. Thus we

Fig. 2. High frequency (dashed line) and quasistatic (solid line) capacitance–voltage curves: (a) sample nitried at 400 °C, (b) sample nitrided at 150 °C.

Fig. 3. Loss \((G/\omega)\) vs angular frequency \((\omega)\) curve for sample nitrided at low temperature at different biases.

Fig. 4. Interface state density distribution across the GaAs band gap for a sample nitrided at low temperature. The solid curve is a Gaussian function fitted to these points.
do not believe that direct damage to GaAs has any responsibility for the degraded performance. The elevated nitridation temperature may have been responsible for the lower quality interface. It is also possible that the Si was completely nitrided in the higher temperature process and that a thin layer of unreacted Si is required for low interface state densities. In all XPS spectra an un-nitrided Si peak was obtained indicating that at least some Si was present at the interface after nitridation. However, the final nitrided Si layers used for the capacitors were not examined prior to plasma deposition of the 270 Å thick silicon nitride cap. Based on the data in Fig. 1, it seems likely that there was a small amount of Si remaining at the GaAs/dielectric interface for processing at 400 °C. However, this was probably less than 1 ML.26 Thus the formation of a direct Si$_3$N$_4$/GaAs interface may have accounted for the degradation.

We conclude that an excellent dielectric with low interface trap density can be produced by partial remote plasma nitridation of a Si epitaxial layer on GaAs. This may then be overcoated with a plasma-deposited nitride to obtain the desired nitride thickness.

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